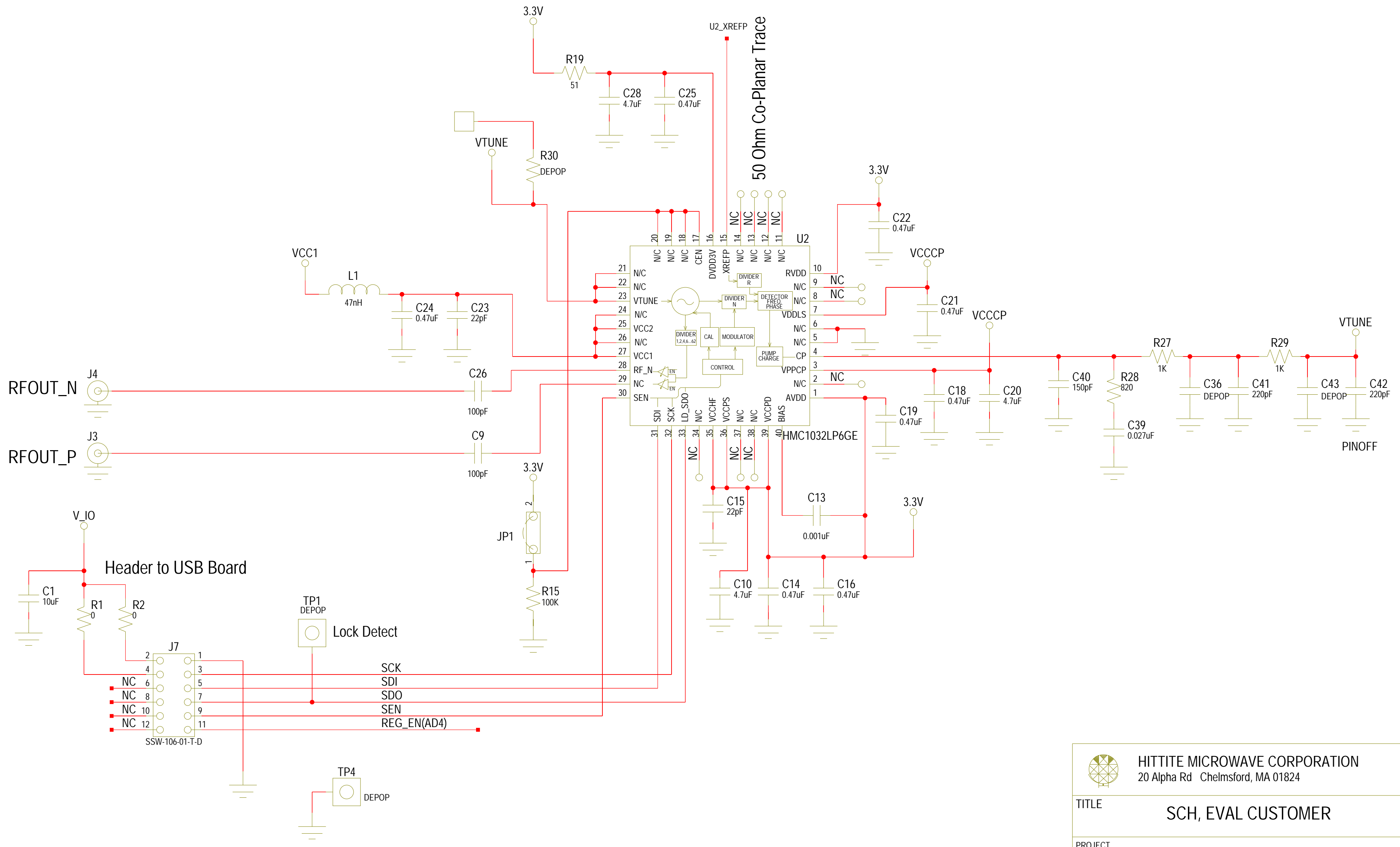



REVISIONS					
REV	ECN#	ZONE	DESCRIPTION	NAME	DATE
D	CP120346	----	CHANGE AS PER CP120346	D. ACEVAL	04/09/2012
E	CP121059	----	CHANGE AS PER CP121059	V. VADUVA	10/04/2012

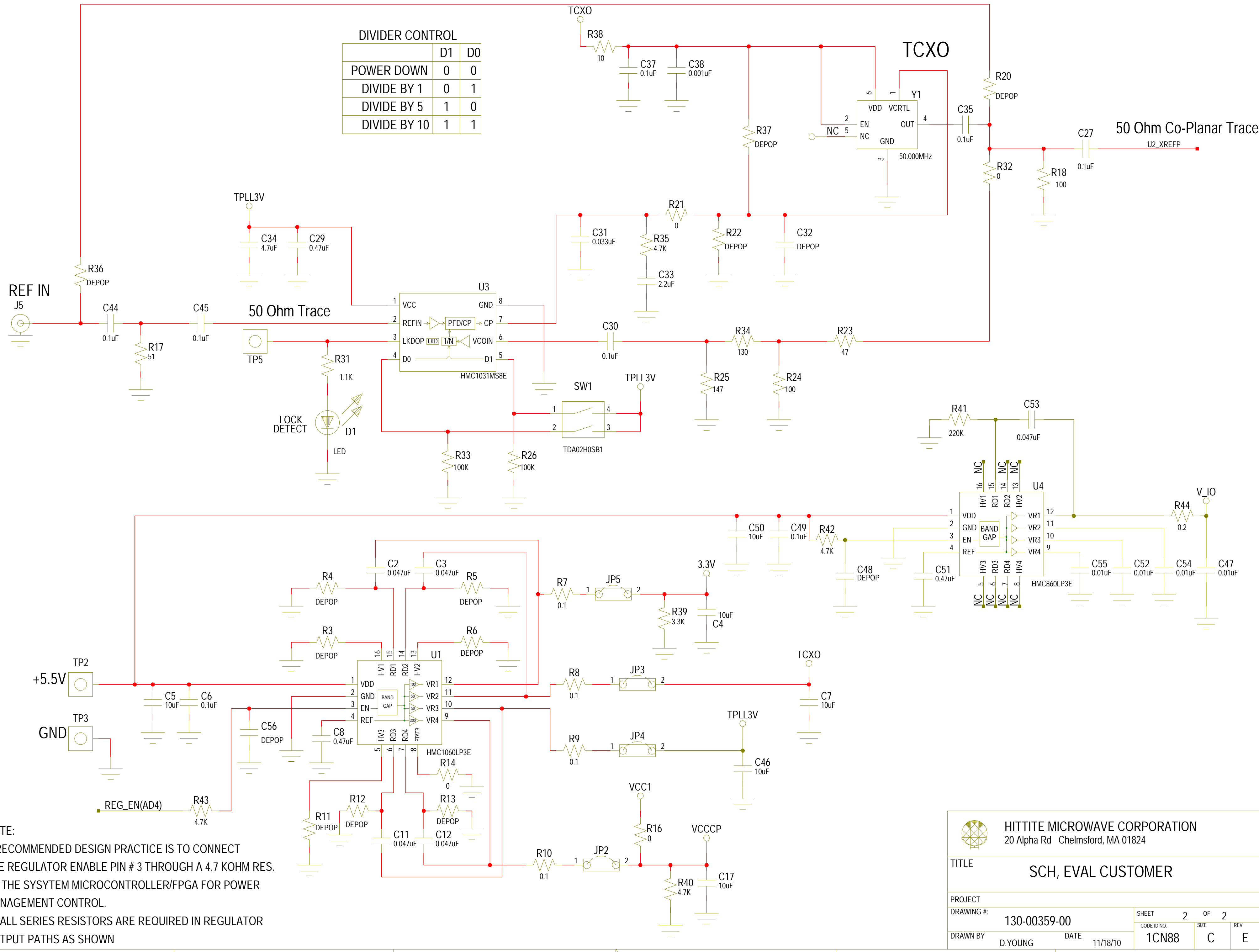
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TITLE SCH, EVAL CUSTOMER				
PROJECT DRAWING #: 130-00359-00				
DRAWN BY: D.YOUNG		DATE: 11/18/10		SHEET 1 OF 2
CODE ID NO.: 1CN88		SIZE: C		REV: E

DIVIDER CONTROL

	D1	D0
POWER DOWN	0	0
DIVIDE BY 1	0	1
DIVIDE BY 5	1	0
DIVIDE BY 10	1	1



NOTE:
 A RECOMMENDED DESIGN PRACTICE IS TO CONNECT THE REGULATOR ENABLE PIN # 3 THROUGH A 4.7 KOHM RES. TO THE SYSYEM MICROCONTROLLER/FPGA FOR POWER MANAGEMENT CONTROL.
 SMALL SERIES RESISTORS ARE REQUIRED IN REGULATOR OUTPUT PATHS AS SHOWN

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TITLE SCH, EVAL CUSTOMER	
PROJECT	
DRAWING #:	130-00359-00
DRAWN BY	D.YOUNG
DATE	11/18/10
SHEET	2 OF 2
CODE ID NO.	1CN88
SIZE	C
REV	E